REMARKS

I. Status of the Application

Claims 15-34 are pending in this application. In the July 29, 2005 office action, the Examiner:

A. Rejected claims 28 and 29 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite;

B. Rejected claims 15-34 under 35 U.S.C. § 103(a) as allegedly being obvious over Foreign Application (JP 6-53 800) in view of Kimura (U.S. Pat. 6,851,849), Hartwick (U.S. Pat. 4,881,024), Kumar (U.S. Pat. 6,855,981) and/or Pavlin (U.S. Pat. 5,438,286).

In this response, applicants have amended claims 15, 24, 28 and 29 and cancelled claim 16. Applicants respectfully traverse the rejections and request reconsideration of the application in view of the foregoing amendments and the following remarks.

II. The Indefiniteness Rejections are Moot

The Examiner rejected claims 28 and 29 as allegedly being indefinite. Claims 28 and 29 have been amended to more distinctly point out the subject matter of the invention. For instance, claim 28 has been amended to say that the first and second MOS transistors comprise CoolMOS transistors. Support for this amendment of claim 28 is found on page 5, lines 14-17 of the specification. Claim 29 has been amended to say "charge compensation regions." Support for this amendment can be found in the specification on page 7, lines 12-15 of the specification. Thus, it is believed that the indefiniteness rejections of claims 28 and 29 are now moot.

III. Obviousness Rejection of Claim 15

Claim 15 stands rejected as allegedly being rendered obvious over the Foreign Application (JP 6-53 800) in view of Pavlin. Claim 15 has been amended to include the limitation of claim 16 that the constant voltage element is a Zener diode. As will be discussed below in detail, the Foreign Application and Pavlin fails to teach, show or suggest each and every element of claim 15. As a consequence, it is respectfully submitted that the obviousness rejection of claim 15 should be withdrawn.

A. Present Invention

Claim 15, as amended, is directed to a MOSFET circuit comprising a first MOS transistor, a second MOS transistor and a Zener diode. The number of cells in the second MOS is less than the number of cells in the first MOS, and the source-drain paths of each transistor are connected in parallel between a voltage source and a reference potential. The Zener diode is coupled between a gate of the first MOS transistor and a gate of the second MOS transistor.

Thus, claim 15, as amended, recites that a Zener diode be used. One characteristic of a Zener diode is that a voltage applied to this element does not further increase above a specific current threshold value. As a consequence, a Zener diode can produce a constant voltage. Because the second MOS transistor has fewer cells than the first MOS transistor, the second transistor switches off after the first MOS transistor when the Zener voltage is applied. Because the Zener output voltage is relatively constant as applied to the first and second MOS transistors, output voltage oscillations are reduced.

B. Foreign Application (JP 6-53 800) nor Pavlin Teach the Use of a Zener Diode

The Foreign Application (JP 6-53 800) was cited as providing the teaching of circuit arrangement having a first and second MOS transistor and a diode. Pavlin was cited to provide the teaching of the first and second MOS transistor having different numbers of cells. However, neither the Foreign Application (JP 6-53 800) nor Pavlin teach the use of a Zener diode as required by applicant's claim 15.

Foreign Application (JP 6-53 800) teaches a circuit arrangement comprising a pair of transistors and a diode "SBD2" provided between the gates of the transistors. Applicant respectfully submits that the examiner has mischaracterized the SBD2 diode as a Zener diode. The "SBD" stands for Schottky-Barrier-Diode. A Shottky diode is not suitable for solving the object of reducing output voltage oscillations because it does not have the characteristic of having a constant voltage output even when there are great fluctuations of the input voltage.

Pavlin was cited for providing the teaching of MOS transistors with different numbers of cells. Similar to the Foreign Application, Pavlin does not teach the use of a Zener diode coupled between the gates of a first and second transistor. In fact, none of the references cited by the examiner, either alone or in combination, teach, show or suggest the use of a Zener diode connected between the gates of two transistors which are connected in parallel to each other and having different numbers of cells.

Thus, the circuit arrangement of the Foreign Application, either alone or in combination with Pavlin or any of the references cited by the examiner, does not teach, show or suggest the limitation of a Zener diode provided between the gates of two transistors connected in parallel having different numbers of cells. Accordingly, it is believed that claim 15, as amended, is patentable over the prior art.

IV. Claims 17-23

Claims 17-23 were rejected as being obvious over Foreign Application (JP 6-53 800) in view of Pavlin, Hartwick, Kimura or Kumar. Claims 17-23 all depend from and incorporate all of the limitations of claim 15. As discussed above, claim 15 is patentable over the Foreign Application (JP 6-53 800), Pavlin, Hartwick, Kimura and Kumar either alone or in combination. Accordingly, it is respectfully submitted that the rejections of claims 17-23 should be withdrawn for at least the same reasons as those set forth above in connection with claim 15.

V. Claims 24 and 30

Claims 24 and 30 stand rejected as allegedly being obvious over the Foreign Application and Pavlin. Claim 24 has been amended to include the limitation of a Zener diode coupled between the gates of the first and second MOS transistors. Claim 30 includes this limitation as originally filed. Accordingly, it is respectfully submitted that the prior art rejections of claims 24 and 30 should be withdrawn for at least the same reasons as those set forth above in connection with claim 15.

VI. Claims 25-29 and 31-34

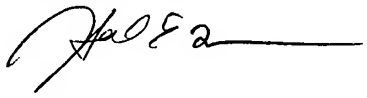
Claims 25-29 and 31-34 were rejected as being obvious over Foreign Application (JP 6-53 800) in view of Pavlin, Hartwick, Kimura or Kumar. Claims 25-29 and 31-34 all depend from and incorporate all of the limitations of their base claims 24 or 30. As discussed above, claims 24 and 30 are patentable over the prior art for at least the same reasons as those set forth above in connection with claim 15. Accordingly, it is respectfully submitted that the

rejections of claims 25-29 and 31-34 should be withdrawn for at least the same reasons as those set forth above in connection with claims 15, 24 and 30.

VII. Conclusion

For all of the foregoing reasons, it is respectfully submitted that the application is in a condition for allowance. Favorable reconsideration and allowance of this application is, therefore, earnestly solicited.

Respectfully Submitted,



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